R4000 Processor Signal Descriptions

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This chapter describes the signals used by and in conjunction with the R4000 processor. The signals include the System interface, the Clock/Control interface, the Secondary Cache interface, the Interrupt interface, the Joint Test Action Group (JTAG) interface, and the Initialization interface.

Signals are listed in bold, and low active signals have a trailing asterisk—for instance, the low-active Read Ready signal is **RdRdy***. The signal description also tells if the signal is an input (the processor receives it) or output (the processor sends it out).

Figure 8-1 illustrates the functional groupings of the processor signals.

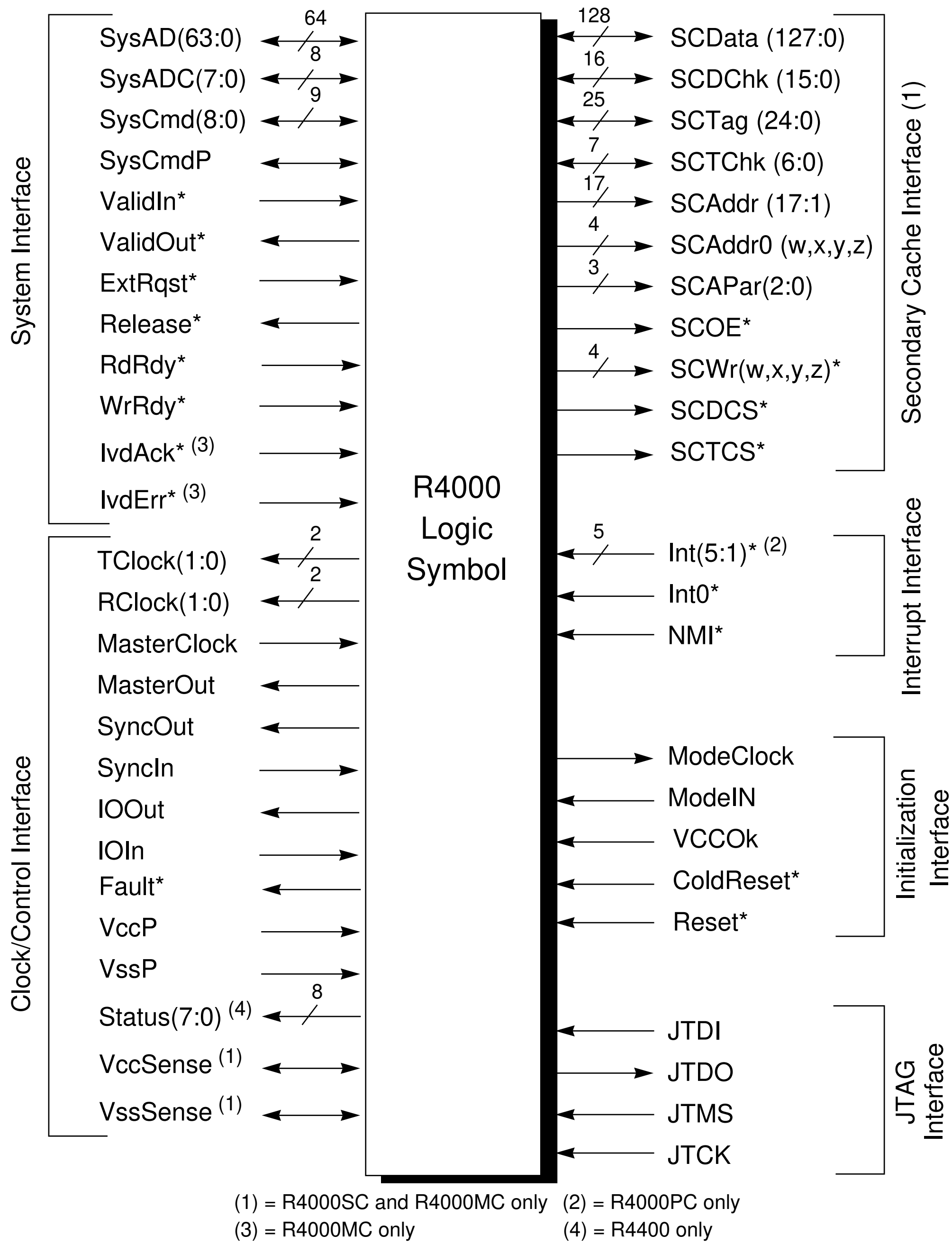

Figure 8-1 R4000 Processor Signals

8.1 System Interface Signals

System interface signals provide the connection between the R4000 processor and the other components in the system. **IvdAck*** and **IvdErr*** signals are applicable only on R4000MC; on the R4000SC they must be tied to Vcc. The remaining signals are available on all three of the package configurations.

Table 8-1 lists the system interface signals.

Table 8-1 System Interface Signals

Name	Definition	Direction	Description
ExtRqst*	External request	Input	An external agent asserts **ExtRqst*** to request use of the System interface. The processor grants the request by asserting **Release***.
IvdAck*	Invalidate acknowledge	Input	An external agent asserts **IvdAck*** to signal successful completion of a processor invalidate or update request (R4000MC only; tie to Vcc on R4000SC).
IvdErr*	Invalidate error	Input	An external agent asserts **IvdErr*** to signal unsuccessful completion of a processor invalidate or update request (R4000MC only; tie to Vcc on R4000SC).
Release*	Release interface	Output	In response to the assertion of **ExtRqst***, the processor asserts **Release***, signalling to the requesting device that the System interface is available.
RdRdy*	Read ready	Input	The external agent asserts **RdRdy*** to indicate that it can accept processor read, invalidate, or update requests in both secondary-cache and no-secondary-cache mode; or can accept a read followed by write request, a read followed by a potential update request, or a read followed by a potential update followed by a write request in secondary cache mode.
SysAD(63:0)	System address/ data bus	Input/ Output	A 64-bit address and data bus for communication between the processor and an external agent.

Table 8-1 (cont.) System Interface Signals

Name	Definition	Direction	Description
SysADC(7:0)	System address/ data check bus	Input/Output	An 8-bit bus containing check bits for the SysAD bus.†
SysCmd(8:0)	System command/ data identifier	Input/Output	A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	System command/ data identifier bus parity	Input/Output	A single, even-parity bit for the SysCmd bus. When the System interface is set to parity mode, the processor also indicates a secondary cache ECC error by corrupting the state of the **SysCmdP** signal.
ValidIn*	Valid input	Input	The external agent asserts **ValidIn*** when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Valid output	Output	The processor asserts **ValidOut*** when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
WrRdy*	Write ready	Input	An external agent asserts **WrRdy*** when it can accept a processor write request.

†. The **SysADC(7:0)** bits map to the SysAD bus in this manner: **SysADC(7)** covers **SysAD(63:56)**, **SysADC(6)** covers **SysAD(55:48)**, and so on down to **SysADC(0)**, which covers **SysAD(7:0)**.

8.2 Clock/Control Interface Signals

The Clock/Control interface signals make up the interface for clocking and maintenance. Table 8-2 lists the Clock/Control interface signals.

Table 8-2 Clock/Control Interface Signals

Name	Definition	Direction	Description
IOOut	I/O output	Output	Output slew rate control feedback loop output. Must be connected to **IOIn** through a delay loop that models the I/O path from the processor to an external agent.
IOIn	I/O input	Input	Output slew rate control feedback loop input (see **IOOut**).
MasterClock	Master clock	Input	Master clock input that establishes the processor operating frequency.
MasterOut	Master clock out	Output	Master clock output aligned with **MasterClock**.
RClock(1:0)	Receive clocks	Output	Two identical receive clocks that establish the System interface frequency.
SyncOut	Synchronization clock out	Output	Synchronization clock output. Must be connected to **SyncIn** through an interconnect that models the interconnect between **MasterOut**, **TClock**, **RClock**, and the external agent.
SyncIn	Synchronization clock in	Input	Synchronization clock input.
TClock(1:0)	Transmit clocks	Output	Two identical transmit clocks that establish the System interface frequency.
Fault*	Fault	Output	The processor asserts **Fault*** to indicate a mismatch output of boundary comparators, and indication of System interface input parity or ECC errors.

Table 8-2 (cont.) Clock/Control Interface Signals

Name	Definition	Direction	Description
Status(7:0)	Status	Output	An 8-bit bus that indicates the current operational status of the processor. R4400 only.
VccP	Quiet Vcc for PLL	Input	Quiet Vcc for the internal phase locked loop.
VccSense	Vcc sense	Input/ Output	A special pin used only in component testing and characterization,**VccSense** provides a separate, direct connection from the on-chip Vcc node to a package pin, without connecting to the in-package power planes. Test fixtures treat **VccSense** as an analog output pin; the voltage at this pin directly exhibits the behavior of the on-chip Vcc. Thus, characterization engineers can easily observe the effects of Δi/Δt noise, transmission line reflections, etc. **VccSense** should be connected to Vcc in functional system designs.
VssP	Quiet Vss for PLL	Input	Quiet Vss for the internal phase locked loop.
VssSense	Vss sense	Input/ Output	**VssSense** provides a separate, direct connection from the on-chip Vss node to a package pin without having to connect to the in-package ground planes. **VssSense** should be connected to Vss in functional system designs.

8.3 Secondary Cache Interface Signals

Secondary Cache interface signals constitute the interface between the R4000 processor and secondary cache. These signals are available only on the R4000MC and R4000SC. Table 8-3 lists the Secondary Cache interface signals.

Table 8-3 Secondary Cache Interface Signals

Name	Definition	Direction	Description
SCAddr(17:1)	Secondary cache address bus	Output	The 18-bit address bus for the secondary cache. Bit 0 has four output lines, (**SCAddr0W:Z**), to provide additional drive current.
SCAddr0W	Secondary cache address LSB	Output	
SCAddr0X	Secondary cache address LSB	Output	
SCAddr0Y	Secondary cache address LSB	Output	
SCAddr0Z	Secondary cache address LSB	Output	
SCAPar(2:0)	Secondary cache address parity bus	Output	A 3-bit bus that carries the parity of the SCAddr bus and the cache control line **SCWr***. The individual bit definitions are:
SCAPar2	Secondary cache address parity bus	Output	Even parity for **SCAddr(17:12)** and **SCWr***
SCAPar1	Secondary cache address parity bus	Output	Even parity for **SCAddr(11:6)** and **SCDCS***
SCAPar0	Secondary cache address parity bus	Output	Even parity for **SCAddr(5:0)** and **SCTCS***
SCData(127:0)	Secondary cache data bus	Input/Output	A 128-bit bus used to read or write cache data from and to the secondary cache data RAM.

Table 8-3 (cont.) Secondary Cache Interface Signals

Name	Definition	Direction	Description
SCDChk(15:0)	Secondary cache data ECC bus	Input/Output	A 16-bit bus that carries two 8-bit ECC fields that cover the 128 bits of SCData from/to secondary cache. **SCDChk(15:8)** corresponds to **SCData(127:64)** and **SCDChk(7:0)** corresponds to **SCData(63:0)**.
SCDCS*	Secondary cache data chip select	Output	Chip select enable signal for the secondary cache data RAM.
SCOE*	Secondary cache output enable	Output	Output enable for the secondary cache data and tag RAM.
SCTag(24:0)	Secondary cache tag bus	Input/Output	A 25-bit bus used to read or write cache tags from and to the secondary cache.
SCTChk(6:0)	Secondary cache tag ECC bus	Input/Output	A 7-bit bus that carries an ECC field covering the SCTag from and to the secondary cache.
SCTCS*	Secondary cache tag chip select	Output	Chip select enable signal for the secondary cache tag RAM.
SCWrW*	Secondary cache write enable	Output	Write enable for the secondary cache data and tag RAM.
SCWrX*	Secondary cache write enable	Output	Write enable for the secondary cache data and tag RAM.
SCWrY*	Secondary cache write enable	Output	Write enable for the secondary cache data and tag RAM.
SCWrZ*	Secondary cache write enable	Output	Write enable for the secondary cache data and tag RAM.

8.4 Interrupt Interface Signals

The Interrupt interface signals make up the interface used by external agents to interrupt the R4000 processor. **Int*(5:1)** are available only on the R4000PC; **Int*(0)** and **NMI*** are available on all three configurations. Table 8-4 lists the Interrupt interface signals.

Table 8-4 Interrupt Interface Signals

Name	Definition	Direction	Description
Int*(5:1)	Interrupt	Input	Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register. R4000PC only.
Int*(0)	Interrupt	Input	One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
NMI*	Nonmaskable interrupt	Input	Nonmaskable interrupt, ORed with bit 6 of the interrupt register.

8.5 JTAG Interface Signals

The JTAG interface signals make up the interface that provides the JTAG boundary scan mechanism. Table 8-5 lists the JTAG interface signals.

Table 8-5 JTAG Interface Signals

Name	Definition	Direction	Description
JTDI	JTAG data in	Input	Data is serially scanned in through this pin.
JTCK	TAG clock input	Input	The processor outputs a serial clock on **JTCK**. On the rising edge of **JTCK**, both **JTDI** and **JTMS** are sampled.
JTDO	JTAG data out	Output	Data is serially scanned out through this pin.
JTMS	JTAG command	Input	JTAG command signal, indicating the incoming serial data is command data.

8.6 Initialization Interface Signals

The Initialization interface signals make up the interface by which an external agent initializes the processor operating parameters. These signals are available on each of the three processor configurations. Table 8-6 lists the Initialization interface signals.

Table 8-6 Initialization Interface Signals

Name	Definition	Direction	Description
ColdReset*	Cold reset	Input	This signal must be asserted for a power on reset or a cold reset. The clocks **SClock**, **TClock**, and **RClock** begin to cycle and are synchronized with the deasserted edge of **ColdReset***. **ColdReset*** must be deasserted synchronously with **MasterOut**.
ModeClock	Boot mode clock	Output	Serial boot-mode data clock output; runs at the system clock frequency divided by 256: (**MasterClock**/256).
ModeIn	Boot mode data in	Input	Serial boot-mode data input.
Reset*	Reset	Input	This signal must be asserted for any reset sequence. It can be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm† reset. **Reset*** must be deasserted synchronously with **MasterOut**.
VCCOk	Vcc is OK	Input	When asserted, this signal indicates to the processor that the +5 volt power supply has been above 4.75 volts for more than 100 milliseconds and will remain stable. The assertion of **VCCOk** initiates the initialization sequence.

†. A warm reset restarts processor, but does not affect clocks; it preserves the processor internal state. A description of warm reset is given in Chapter 9.

8.7 Signal Summary

Table 8-7 R4000SC/MC Processor Signal Summary

Description	Name	I/O	Asserted State	3-State
Secondary cache data bus	SCData(127:0)	I/O	High	Yes
Secondary cache data ECC bus	SCDChk(15:0)	I/O	High	Yes
Secondary cache tag bus	SCTag(24:0)	I/O	High	Yes
Secondary cache tag ECC bus	SCTChk(6:0)	I/O	High	Yes
Secondary cache address bus	SCAddr(17:1)	O	High	No
Secondary cache address LSB	SCAddr0Z	O	High	No
Secondary cache address LSB	SCAddr0Y	O	High	No
Secondary cache address LSB	SCAddr0X	O	High	No
Secondary cache address LSB	SCAddr0W	O	High	No
Secondary cache address parity bus	SCAPar(2:0)	O	High	No
Secondary cache output enable	SCOE*	O	Low	No
Secondary cache write enable	SCWrZ*	O	Low	No
Secondary cache write enable	SCWrY*	O	Low	No
Secondary cache write enable	SCWrX*	O	Low	No
Secondary cache write enable	SCWrW*	O	Low	No
Secondary cache data chip select	SCDCS*	O	Low	No
Secondary cache tag chip select	SCTCS*	O	Low	No
System address/data bus	SysAD(63:0)	I/O	High	Yes
System address/data check bus	SysADC(7:0)	I/O	High	Yes
System command/data identifier bus	SysCmd(8:0)	I/O	High	Yes
System command/data identifier bus parity	SysCmdP	I/O	High	Yes
Valid input	ValidIn*	I	Low	No
Valid output	ValidOut*	O	Low	No
External request	ExtRqst*	I	Low	No
Release interface	Release*	O	Low	No
Read ready	RdRdy*	I	Low	No
Write ready	WrRdy*	I	Low	No
Invalidate acknowledge	IvdAck*	I	Low	No
Invalidate error	IvdErr*	I	Low	No

Table 8-7 (cont.) R4000SC/MC Processor Signal Summary

Description	Name	I/O	Asserted State	3-State
Interrupt	Int*(0)	I	Low	No
Nonmaskable interrupt	NMI*	I	Low	No
Boot mode data in	ModeIn	I	High	No
Boot mode clock	ModeClock	O	High	No
JTAG data in	JTDI	I	High	No
JTAG data out	JTDO	O	High	No
JTAG command	JTMS	I	High	No
JTAG clock input	JTCK	I	High	No
Transmit clocks	TClock(1:0)	O	High	No
Receive clocks	RClock(1:0)	O	High	No
Master clock	MasterClock	I	High	No
Master clock out	MasterOut	O	High	No
Synchronization clock out	SyncOut	O	High	No
Synchronization clock in	SyncIn	I	High	No
I/O output	IOOut	O	High	No
I/O input	IOIn	I	High	No
Vcc is OK	VCCOk	I	High	No
Cold reset	ColdReset*	I	Low	No
Reset	Reset*	I	Low	No
Fault	Fault*	O	Low	No
Quiet Vcc for PLL	VccP	I	High	No
Quiet Vss for PLL	VssP	I	High	No
Status	Status(7:0)	O	High	No
Vcc sense	VccSense	I/O	N/A	No
Vss sense	VssSense	I/O	N/A	No

Table 8-8 R4000PC Processor Signal Summary

Description	Name	I/O	Asserted State	3-State
System address/data bus	SysAD(63:0)	I/O	High	Yes
System address/data check bus	SysADC(7:0)	I/O	High	Yes
System command/data identifier bus	SysCmd(8:0)	I/O	High	Yes
System command/data identifier bus parity	SysCmdP	I/O	High	Yes
Valid input	ValidIn*	I	Low	No
Valid output	ValidOut*	O	Low	No
External request	ExtRqst*	I	Low	No
Release interface	Release*	O	Low	No
Read ready	RdRdy*	I	Low	No
Write ready	WrRdy*	I	Low	No
Interrupts	Int*(5:1)	I	Low	No
Interrupt	Int*(0)	I	Low	No
Nonmaskable interrupt	NMI*	I	Low	No
Boot mode data in	ModeIn	I	High	No
Boot mode clock	ModeClock	O	High	No
JTAG data in	JTDI	I	High	No
JTAG data out	JTDO	O	High	No
JTAG command	JTMS	I	High	No
JTAG clock input	JTCK	I	High	No
Transmit clocks	TClock(1:0)	O	High	No
Receive clocks	RClock(1:0)	O	High	No
Master clock	MasterClock	I	High	No
Master clock out	MasterOut	O	High	No
Synchronization clock out	SyncOut	O	High	No
Synchronization clock in	SyncIn	I	High	No
I/O output	IOOut	O	High	No
I/O input	IOIn	I	High	No
Vcc is OK	VCCOk	I	High	No

Table 8-8 (cont.)   R4000PC Processor Signal Summary

Description	Name	I/O	Asserted State	3-State
Cold reset	ColdReset*	I	Low	No
Reset	Reset*	I	Low	No
Fault	Fault*	O	Low	No
Quiet Vcc for PLL	VccP	I	High	No
Quiet Vss for PLL	VssP	I	High	No