18. Cache Test Mode

The R10000 processor provides a cache test mode that may be used during manufacturing test and system debug to access the following internal RAM arrays:

- data cache data array
- data cache tag array
- instruction cache data array
- instruction cache tag array
- secondary cache way predication table

18.1 Interface Signals

Cache test mode is accessed by using a subset of the system interface signals. By not requiring the use of any secondary cache interface signals, the internal RAM arrays may be accessed for single-chip LGA as well as R10000/secondary cache module configurations.

The following system interface signals are used during cache test mode:

- **SysAD(57:0)**
- **SysVal***

Any input signals not listed above are ignored by the processor when it is operating in cache test mode, and any output signals not listed above are undefined during cache test mode.

18.2 System Interface Clock Divisor

Cache test mode is supported for all system interface clock speeds. However, since cache test mode repeat rates and latencies are expressed in terms of **PClk** cycles, the external agent must take care when operating at any system interface clock divisor other than Divide-by-1.

18.3 Entering Cache Test Mode

In order for the processor to enter cache test mode, the external agent must begin a Power-on or Cold Reset sequence.

Rather than negating **SysReset*** at the end of the reset sequence, the external agent loads the mode bits into the processor by driving the mode bits (with the **CTM** signal asserted) on **SysAD(63:0)**, waits at least two **SysClk** cycles, and then asserts **SysGnt*** for at least one **SysClk** cycle.

After waiting at least another 100 ms, the external agent may issue the first cache test mode command.

Figure 18-1 shows the cache test mode entry sequence.

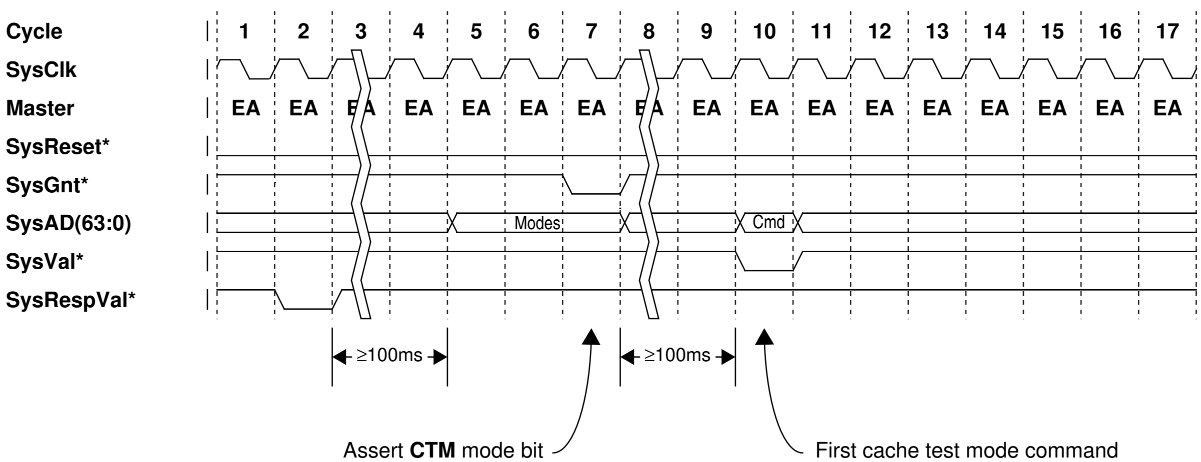

Figure 18-1 Cache Test Mode Entry Sequence

18.4 Exit Sequence

To leave cache test mode, the external agent does the following:

- loads the mode bits into the processor by driving the mode bits (with the **CTM** mode bit negated) on **SysAD(63:0)**
- waits at least two **SysClk** cycles
- asserts **SysGnt*** for at least one **SysClk** cycle

After at least one **SysClk** cycle, the external agent may negate **SysReset*** to end the reset sequence.

Figure 18-2 shows the cache test mode exit sequence.

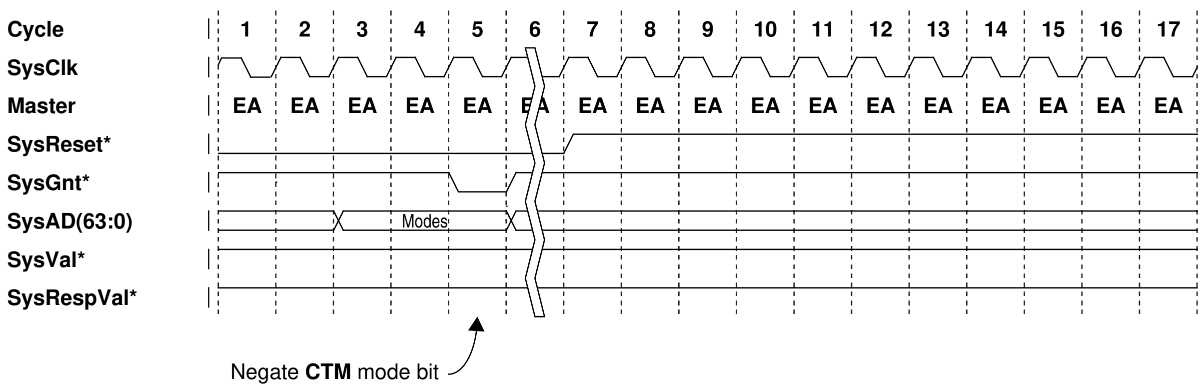

Figure 18-2 Cache Test Mode Exit Sequence

18.5 SysAD(63:0) Encoding

Encoding of the **SysAD(63:0)** bus during cache test mode is shown in Table 18-1. “Unused” fields are read as “undefined,” and must be written as zeroes.

Table 18-1 Cache Test Mode **SysAD(63:0)** *Encoding*

<table>
<tr><th>SysAD Bit</th><th>Data Cache Data Array</th><th>Data Cache Tag Array</th><th>Instruction Cache Data Array</th><th>Instruction Cache Tag Array</th><th>Secondary Cache Way Predication Array</th></tr>
<tr><td>0</td><td rowspan="9">Data</td><td>Tag parity</td><td rowspan="10">Data</td><td>Tag parity</td><td>MRU</td></tr>
<tr><td>1</td><td>SCWay</td><td>Unused</td><td rowspan="12">Unused</td></tr>
<tr><td>2</td><td>State parity</td><td>State parity</td></tr>
<tr><td>3</td><td>LRU</td><td>LRU</td></tr>
<tr><td>4</td><td rowspan="2">Unused</td><td rowspan="2">Unused</td></tr>
<tr><td>5</td></tr>
<tr><td>6</td><td rowspan="2">State</td><td>State</td></tr>
<tr><td>7</td><td>Unused</td></tr>
<tr><td>31:8</td><td rowspan="2">Tag</td><td rowspan="2">Tag</td></tr>
<tr><td>35:32</td><td>Data parity</td></tr>
<tr><td>36</td><td rowspan="3">Unused</td><td rowspan="2">StateMod</td><td>Data parity</td><td rowspan="3">Unused</td></tr>
<tr><td>38:37</td><td rowspan="2">Unused</td></tr>
<tr><td>39</td><td>Unused</td></tr>
<tr><td rowspan="2">42:40</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
<tr><td colspan="5">Array select</td></tr>
<tr><td>43</td><td colspan="5">Write/Read select</td></tr>
<tr><td>44</td><td colspan="5">Auto-increment select</td></tr>
<tr><td>45</td><td colspan="5">Way</td></tr>
<tr><td>57:46</td><td colspan="5">Address</td></tr>
<tr><td>63:58</td><td colspan="5">Unused</td></tr>
</table>

18.6 Cache Test Mode Protocol

This section describes the cache test mode protocol in detail, including:

- normal write protocol
- auto-increment protocol
- normal read protocol
- auto-increment read protocol

Normal Write Protocol

A cache test mode **normal write** operation writes a selected RAM array. The write address, way, array, and data are specified in the write command.

The external agent issues a normal write command by:

- driving the address on **SysAD(57:46)**
- driving the way on **SysAD(45)**
- negating the auto-increment select on **SysAD(44)**
- asserting the Write/Read select on **SysAD(43)**
- driving the array select on **SysAD(42:40)**
- driving the write data on **SysAD(39:0)**
- asserting **SysVal*** for one **SysClk** cycle

Normal writes have a repeat rate of 8 **PClk** cycles.

Figure 18-3 depicts two cache test mode normal writes.

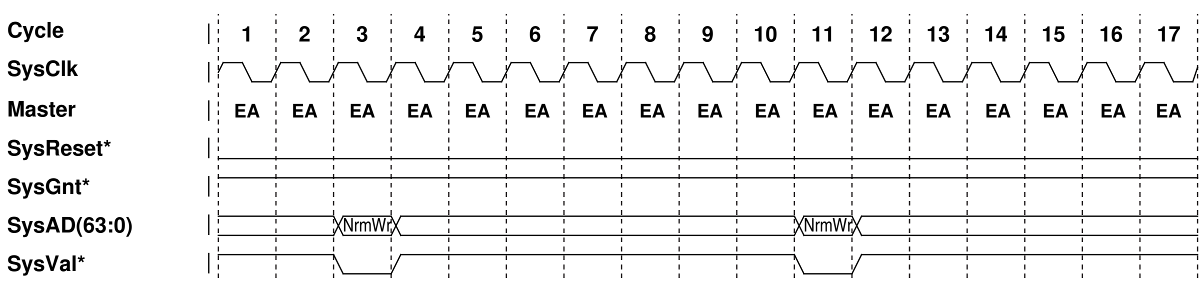

Figure 18-3 Cache Test Mode Normal Write Protocol

Auto-Increment Write Protocol

A cache test mode **auto-increment write** operation writes a selected RAM array. The write address is obtained by incrementing the previous write address, and the write way is obtained from the previous write way.

If an overflow occurs when incrementing the previous write address, the address wraps to 0, and the way is toggled.

The write data is identical to the previous write data.

For proper results, an auto-increment write must always be proceeded by a normal or auto-increment write.

The external agent issues an auto-increment write command by:

- asserting the auto-increment select on **SysAD(44)**
- asserting the Write/Read select on **SysAD(43)**
- driving the array select on **SysAD(42:40)**
- asserting **SysVal*** for one **SysClk** cycle

Auto-increment writes have a repeat rate of one **PClk** cycle.

Figure 18-4 depicts three cache test mode auto-increment writes.

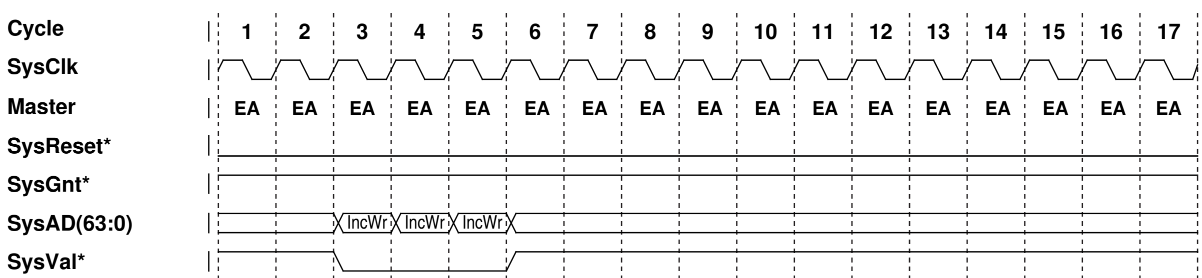

Figure 18-4 Cache Test Mode Auto-Increment Write Protocol

Normal Read Protocol

A cache test mode **normal read** operation reads a selected RAM array. The read address, way, and array are specified by the read command.

The external agent issues a normal read command by:

- driving the address on **SysAD(57:46)**
- driving the way on **SysAD(45)**
- negating the auto-increment select on **SysAD(44)**
- negating the Write/Read select on **SysAD(43)**
- driving the array select on **SysAD(42:40)**
- asserting **SysVal*** for one **SysClk** cycle.

After a read latency of 15 **PClk** cycles, the processor provides the read response by:

- entering *Master* state
- driving the read data on **SysAD(39:0)**
- asserting **SysVal*** for one **SysClk** cycle.

In the following **SysClk** cycle, the processor reverts to *Slave* state.

Normal reads have a repeat rate of 17 **PClk** cycles.

Figure 18-5 depicts two cache test mode normal reads.

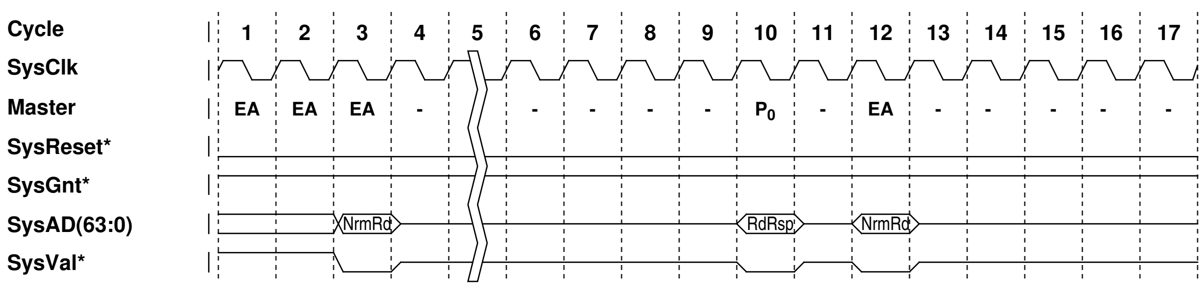

Figure 18-5 Cache Test Mode Normal Read Protocol

Auto-Increment Read Protocol

A cache test mode **auto-increment read** operation reads a selected RAM array. The read address is obtained by incrementing the previous access address, and the read way is obtained from the previous access way.

If an overflow occurs when incrementing the previous access address, the address wraps to 0, and the way is toggled.

The external agent issues an auto-increment read command by:

- asserting the auto-increment select on **SysAD(44)**
- negating the Write/Read select on **SysAD(43)**
- driving the array select on **SysAD(42:40)**
- asserting **SysVal*** for one **SysClk** cycle.

After a read latency of 15 **PClk** cycles, the processor provides the read response by:

- entering *Master* state
- driving the read data on **SysAD(39:0)**
- asserting **SysVal*** for one **SysClk** cycle.

In the following **SysClk** cycle, the processor reverts to *Slave* state.

Auto-increment reads have a repeat rate of 17 **PClk** cycles.

Figure 18-6 depicts two cache test mode auto-increment reads.

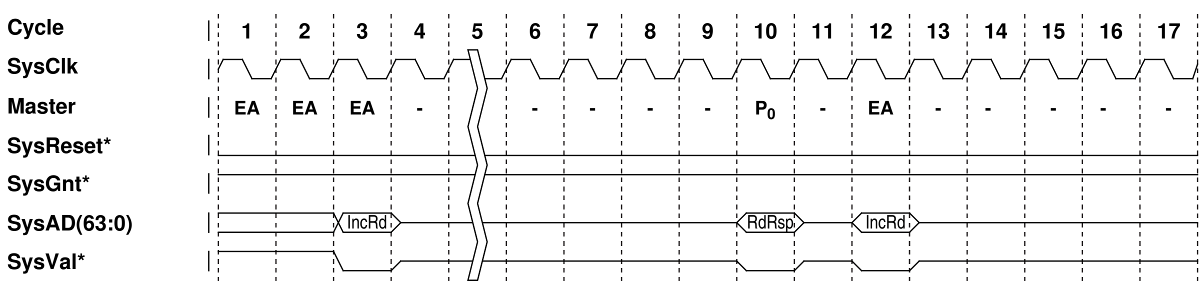

Figure 18-6 Cache Test Mode Auto-Increment Read Protocol