# 12. Electrical Specifications

This chapter contains the following electrical and signal information about the R10000 processor:

- DC electrical specification
- AC electrical specification
- signal integrity issues

## 12.1 DC Electrical Specification

This section describes the following DC electrical characteristics of the R10000 processor:

- DC power supply levels
- **DCOk** and power supply sequencing
- maximum operating conditions
- input signal level sensing
- mode definitions
- **Vref[SC,Sys]**
- unused inputs
- DC input/output specifications

### DC Power Supply Levels

The processor core is powered by a +3.3V (+/- 5%) supply. The processor output drivers are powered from a separate supply, dependent on the output logic family used in the application system:

- For JEDEC-compatible HSTL operation, the nominal value for **VccQSC** and **VccQSys** are in the 1.5V (+/- 100 millivolt) range.
- For CMOS/TTL compatible systems, **VccQSC** and **VccQSys** can be externally tied to the same **Vcc** as the core power supply.

**NOTE:** The I/O pins of the R10000 processor may not be driven higher than 4.0V by any device in the system until the **Vcc** and **VccQ** inputs are stable.

## DCOk and Power Supply Sequencing

The following guidelines are designed to protect the processor from damage or latch-up:

- With respect to the **Vcc** (3.3V) (supply to the core), **VccQ[SC,Sys]** (either 1.5V or 3.3V) must not be driven more than a diode threshold voltage.
- **Vref** should not go higher than **VccQ[SC,Sys]**. Generally, **Vref** is derived from **VccQ** through a resistor divider, and therefore cannot rise above **VccQ**.
- The power to termination resistors must not arrive before **Vcc** and **VccQ[SC,Sys]** arrive at the processor.
- None of the supplies can float or be driven negative.

One method of protecting the processor from excessive input voltage is to sequence the power supplies for the entire system, ensuring that the power to the processor is stable before any components drive signals to the processor. Another method to tristate all external drivers to the processor with the **DCOk** pin, until the processor has stabilized.

> **NOTE:** The input voltage required for the **DCOk** is 3.3V in either the CMOS/TTL or the HSTL configuration. Both **DCOk** pins must be tied together externally.

## Maximum Operating Conditions

Table 12-1 shows the maximum conditions under which the processor operates.

*Table 12-1 Maximum Operating Conditions*

| Parameter | Symbol | Value |
|---|---|---|
| Core Supply Voltage | Vcc | 3.6 volts |
| Output Supply Voltage | VccQ (HTSL)<br>VccQ (CMOS/TTL) | 1.6 volts<br>3.6 volts |
| Junction Temperature | $T_j$ | $20^\circ$ to $85^\circ$ C |
| Applied Input Voltage: | Vin | -0.5 to Vcc+0.5 volts |
| Maximum Power | $P_{R10000}$ | 30 watts |
| **PClk** Frequency | f | 200 MHz |

## Input Signal Level Sensing

The processor input signals are all received by CMOS receivers that are compatible with either HSTL or CMOS/TTL logic levels. The I/O levels are defined by **VrefSC** and **VrefSys**, according to the appropriate logic family (HSTL or CMOS/TTL).

## Mode Definitions

The mode bit, **ODrainSys**, is provided to select the characteristics of the pad ring.

When asserted, this mode bit tristates the PMOS pullup devices to select system interface output drivers. This mode is included to allow for multiprocessor systems to use a GTL-like open drain configuration with external load/termination resistors providing logic high levels.

## Vref[SC,Sys]

The **Vref[SC,Sys]** pins must be connected to a stable reference voltage source. This reference point is used in the input sense amp current mirror to provide the switch point for the logic levels.

Inside the processor, the **Vref[SC,Sys]** signals have a large capacitance, and a low-pass filter at each receiver. The **DCOk** pins must not be asserted until there has been sufficient time for **Vref[SC,Sys]** to stabilize at each of the receivers inside the processor.

A typical **Vref[SC,Sys]** generator is two resistors which provide the **Vref[SC,Sys]** level associated with the chosen logic family, and a 10µF tantalum capacitor connected to the processor's **Vref[SC,Sys]** pin to provide stability.

## Unused Inputs

Several input pins are unused during normal system operation, and should be tied to **Vcc** through resistors:

- **JTDI**
- **JTCK**
- **JTMS**

Several input pins are unused during normal system operation, and should be tied to **Vss** through 100 ohm resistors:

- **TCA, TCB**
- **PLLDis**
- **Spare1, Spare3**

Several input pins are unused during normal system operation, and should be tied to **Vss**:

- **PLLSpare1, PLLSpare2, PLLSpare3, PLLSpare4**
- **SelDVCO**

The following input pins may be unused in certain system configurations, and each of them should be tied to **VccQSys**, preferably, through a resistor of 100 ohms or greater value:

- **SysNMI***

The following input pins may be unused in certain system configurations, and each of them should be tied to **Vss**, preferably, through a resistor of 100 ohms or greater value:

- **SysRdRdy***
- **SysWrRdy***
- **SysGblPerf***
- **SysCyc***

The following input pins may be unused in certain system configurations, and each of them should be tied (preferably) to **Vss**, or **VccQSys**, through a resistor of 100 ohms or greater value:

- **SysADChk(7:0)**

(See page 198 in Errata)

## DC Input/Output Specifications

All processor output drivers are CMOS push-pull, and the signals swing between **VccQ** and **Vss**. In open drain mode, the gates of the PMOS pullup devices are disabled. Input-only pins include a disabled output buffer for implicit ESD protection.

Tables 12-2 and 12-3 describe the DC characteristics of the I/O signals for the HSTL and CMOS/TLL configurations.

> **NOTE:** As the JEDEC Standard 8-x evolves, the HSTL specifications will also change, and the processor will remain compliant with these standards.

*Table 12-2 DC Characteristics for HSTL Configuration*

| Symbol | Parameter | Minimum | Maximum | Units | Conditions |
|---|---|---|---|---|---|
| VOH | Output high voltage | VccQ /2 + 0.3V | N/A | V | N/A |
| VOL | Output low voltage | | VccQ /2 - 0.3V | V | N/A |
| VIH | Input high voltage | Vref + 100mV | Vcc + 300mV | V | N/A |
| VIL | Input low voltage | -300mV | Vref - 100mV | V | N/A |
| ILeak | I/O leakage current | -TBD | TBD | µA | N/A |

*Table 12-3 DC Characteristics for CMOS/TTL Configuration*

| Symbol | Parameter | Minimum | Maximum | Units | Conditions |
|---|---|---|---|---|---|
| VOH | Output high voltage | 2.4 | N/A | V | Vcc = VccQ = min |
| VOL | Output low voltage | N/A | 0.4 | V | Vcc = VccQ = min |
| VIH | Input high voltage | 2.0 | N/A | V | N/A |
| VIL | Input low voltage | N/A | 0.8 | V | N/A |
| ILeak | I/O leakage current | -TBD | TBD | µA | N/A |

## 12.2 AC Electrical Specification

This section describes the following AC electrical characteristics of the R10000 processor:

- maximum operating conditions
- test specification
- secondary cache and system interface timing
- enable/output delay, setup, hold time
- asynchronous inputs

### Maximum Operating Conditions

The R10000 chip clamps signals that overshoot the DC limits established for input logic levels. These limits are published as part of the fabrication process characterization.

The R10000 chip provides silicon diode clamps on all signal pins.

### Test Specification

HSTL test conditions are based on the JEDEC Standard conditions.

### Secondary Cache and System Interface Timing

Timing measurements are referenced from the mid-swing point of the input signal to the crossing point of the **SysClk** and **SysClk*** input clocks. All input signals maintain a 1 V/ns edge rate in the 20% to 80% range of the input signal swing.

## Enable/Output Delay, Setup, Hold Time

Table 12-4 lists the delay, setup, and hold times for the HTSL version of the processor.

*Table 12-4 AC Characteristics for HSTL Configuration*

| HSTL | Minimum | Maximum |
|---|---|---|
| Output delay | 0.5 ns | 1.5 ns |
| Setup | 1.0 ns | |
| Hold | 1.0 ns | |

Table 12-5 lists the delay, setup, and hold times for the CMOS/TTL version of the processor.

*Table 12-5 AC Characteristics for CMOS/TTL Configuration*

| LVCMOS | Minimum | Maximum |
|---|---|---|
| Output delay | 0.5 ns | 2.0 ns |
| Setup | 1.0 ns | |
| Hold | 1.0 ns | |

## Asynchronous Inputs

The **SysReset*** input can be asserted asynchronously to **SysClk**, but must be negated synchronously with **SysClk**, adhering to the AC electrical specifications listed above.

## 12.3 Signal Integrity Issues

In this section, the following signal integrity considerations are described for a R10000-based system:

- Power Supply Regulation
- Decoupling Capacitance
- Reference Voltage
- Maximum Input Voltage Levels
- Output I-V Curves
- Switching and Slew Rate Characteristics

### Reference Voltage

Most input pins on the processor use a current-mirror sense amp with **Vref[SC,Sys]** supplied to the negative input to provide a single rail input receiver. The following input pins are exceptions to this rule:

- **SysClk** and **SysClk***
- **DCOk**

All other inputs require a stable **Vref[SC,Sys]** supply for proper operation.

The **Vref[SC,Sys]** source can be a simple voltage divider; the actual impedance of this source is not critical, since the **Vref[SC,Sys]** signals are sampled through a low-pass filter on the processor.

### Power Supply Regulation

The system must provide connections to all of the **Vcc**, **VccQ[SC,Sys]**, and **Vss** pins on the processor package. The power supply voltages must be held to 5% tolerance at the processor pin connection.

### Maximum Input Voltage Levels

Maximum excursion of the input signal due to ringing may reach Vcc+0.5V or Vss-0.5V for periods of less than 10% of the total driven waveform period. The R10000 processor includes overshoot clamps by silicon diode protection which limit the overshoot to approximately 500 mV beyond each supply rail.

## Decoupling Capacitance

In order to regulate the transient current requirements of a R10000-based system, it is suggested that explicit decoupling capacitors be used. The R10000 package allows for the following capacitors:

- eight **Vcc-Vss**
- five **VccQSC-Vss**
- four **VccQSys-Vss** (See page 203 in Errata)

The package also provides six connections for the PLL power supplies and loop capacitors.

**VccPa** (**VccPd**) is connected to **VssPa** (**VssPd**) through three decoupling capacitors, as shown in Figures 12-1 and 12-2. The 0.1µF and 1 nF low-inductance capacitors are placed in parallel with the 10 µF capacitor, as close to the R10000 package as possible.†

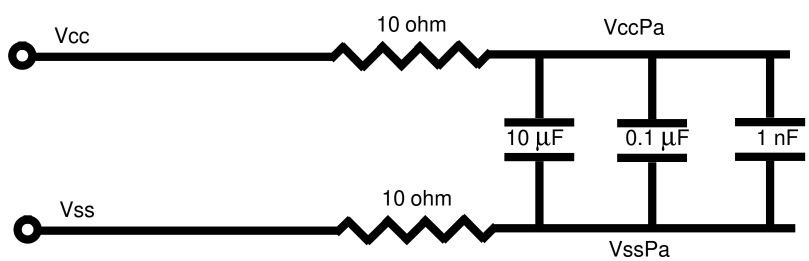


*Figure 12-1 Decoupling VccPa and VssPa*

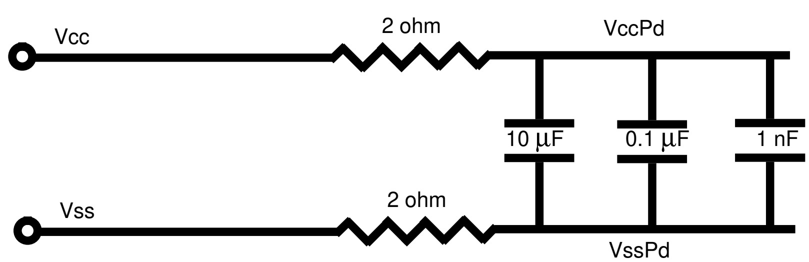


*Figure 12-2 Decoupling VccPd and VssPd*

† Decoupling between VccPa and VssPa is far more important than decoupling between VccPd and VssPd, if both are not possible.

## Output I-V Curves

*Not yet available*

## Switching and Slew Rate Characteristics

*Not yet available*