Clock Signals

7

The R10000 processor has differential PECL clock inputs, SysClk and SysClk*, from which all processor internal clock signals and secondary cache clock signals are derived.

Three major clock domains are in the processor:

- the System interface clock domain, which operates at the system clock frequency and controls the System interface signals
- the internal processor clock domain, which controls the processor core logic
- the secondary cache clock domain, which controls signals communicating with the external secondary cache synchronous SRAM

These domains are described in this chapter.

7.1 System Interface Clock and Internal Processor Clock Domains

In high performance systems, PECL-level differential clocks are routinely used to minimize system clock skews. The R10000 processor receives differential system clock signals at the SysClk and SysClk* pins; two additional pins, SysClkRet and SysClkRet*, are the return paths for termination of these signals.

SysClk and SysClk* are used to drive an on-chip phase-locked loop (PLL), which multiplies the system clock to create an internal processor clock, PClk.

The R10000 processor always communicates with the system at the SysClk frequency, and PClk always runs at a frequency-multiple of SysClk, according to the following formula:

```
PClk = SysClk*(SysClkDiv+1)/2
```

For example, in a 50 MHz system with SysClkDiv = 7 and SCClkDiv =2, PClk = 50*8/2 = 200 MHz.

> NOTE: It is preferred that the R10000 processor uses a differential PECL clock input. However, in a less-aggressive system, a CMOS/TTL single-ended clock can be used to drive the processor, provided its complementary clock input, SysClk*, is tied to an appropriate reference voltage (1.4V for TTL, Vcc/2 for CMOS). In any case, the reference voltage applied to SysClk* should not be less than 1.2V.

7.2 Secondary Cache Clock

The processor uses registered synchronous SRAMs for its secondary cache, to allow pipelined accesses.

The processor provides 6 pairs of differential HSTL clock outputs, SCClk(5:0) and SCClk*(5:0), to be used by the secondary cache synchronous SRAMs. The SCClkTap mode bits (mode bits are described in Chapter 8) specify the alignment of SCClk(5:0) and SCClk*(5:0) relative to the internal secondary cache clock. Note that the output buffer delay is not included.

The secondary cache interface clock is generated by dividing down the internal processor clock, PClk.

SCClk is related to SysClk according to the following formula:

```
SCClk = SysClk*(SysClkDiv+1)/(SCClkDiv+1)
```

For example, in a 50 MHz system with SysClkDiv =7 and SCClkDiv =2, SCClk = 50*8/3 = 133 MHz.

7.3 Phase-Locked-Loop

The processor uses the internal PLL for clock generation and multiplication as shown in Figure 7-1.

Values of the termination resistors for the SysClkRet/SysClkRet* signals are system-dependent. The system designer must select a value based upon the characteristic impedance of the board, therefore it is beyond the scope of this manual to specify values for these termination resistors.

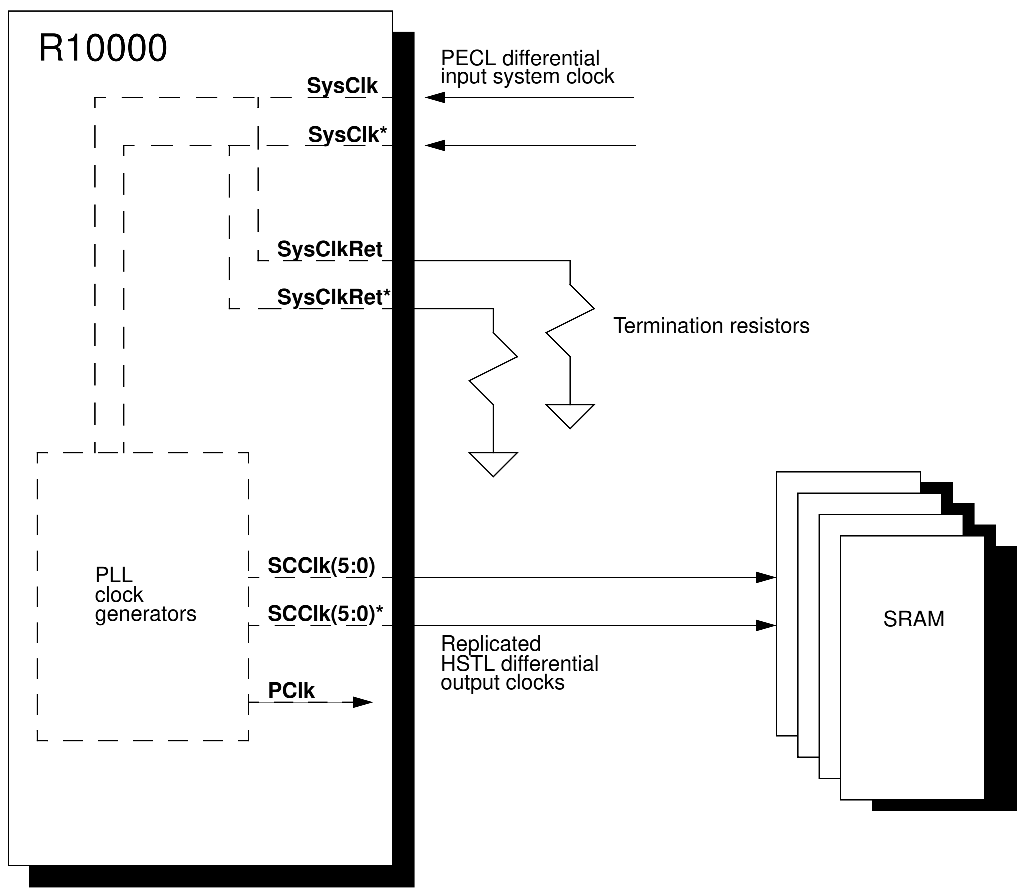

Figure 7-1 R10000 System and Secondary Cache Clock Interface