Interface Signal Descriptions

3

This chapter gives a list and description of the interface signals.

The R10000 interface signals may be divided into the following groups:

- Power interface
- Secondary Cache interface
- System interface
- Test interface

The following sections present a summary of the external interface signals for each of these groups. An asterisk (*) indicates signals that are asserted as a logical 0.

3.1 Power Interface Signals

Table 3-1 presents the R10000 processor power interface signals.

Table 3-1 Power Interface Signals

Signal Name	Description	Type
Vcc	Vcc core Vcc for the core circuits.	Input
VccQSC	Vcc output driver secondary cache Vcc for the secondary cache interface output drivers.	Input
VccQSys	Vcc output driver system Vcc for the System interface output drivers.	Input
VrefSC	Voltage reference secondary cache Voltage reference for the secondary cache interface input receivers.	Input
VrefSys	Voltage reference system Voltage reference for the System interface input receivers.	Input
VrefByp	Voltage reference bypass This pin must be tied to VrefSys or Vss .	Input
Vss	Vss Vss for the core circuits and output drivers.	Input
VccPa	Vcc PLL analog Vcc for the PLL analog circuits.	Input
VssPa	Vss PLL analog Vss for the PLL analog circuits.	Input
VccPd	Vcc PLL digital Vcc for the PLL digital circuits.	Input
VssPd	Vss PLL digital Vss for the PLL digital circuits.	Input
DCOk	DC voltages are OK The external agent asserts these two signals when Vcc , VccQ[SC,Sys] , Vref[SC,Sys] , Vcc[Pa,Pd] , and SysClk are stable.	Input

3.2 Secondary Cache Interface Signals

Table 3-2 presents the R10000 processor secondary cache interface signals.

Table 3-2 Secondary Cache Interface Signals

Signal Name	Description	Type
	SSRAM * Clock Signals	
SCClk(5:0) SCClk*(5:0)	Secondary cache clock Duplicated complementary secondary cache clock outputs.	Output
	SSRAM Address Signals	
SCAAddr(18:0) SCBAddr(18:0)	Secondary cache address bus Duplicated complementary 19-bit bus which specifies the set address of the secondary cache data and tag SSRAM that is to be accessed.	Output
SCTagLSBAddr	Secondary cache tag LSB address Signal that specifies the least significant bit of the address for the secondary cache tag SSRAM.	Output
	SSRAM Data Signals	
SCADWay SCBDWay	Secondary cache data way Duplicated signal that indicates the way of the secondary cache data SSRAM that is to be accessed.	Output
SCData(127:0)	Secondary cache data bus 128-bit bus to read/write cache data from/to secondary cache data SSRAM.	Bidirectional
SCDataChk(9:0)	Secondary cache data check bus A 10-bit bus used to read/write ECC and even parity from/to the secondary cache data SSRAM.	Bidirectional
SCADOE* SCBDOE*	Secondary cache data output enable Duplicated signal that enables the outputs of the secondary cache data SSRAM.	Output
SCADWr* SCBDWr*	Secondary cache data write enable Duplicated signal that enables writing the secondary cache data SSRAM.	Output
SCADCS* SCBDCS*	Secondary cache data chip select Duplicated signal that enables the secondary cache data SSRAM.	Output
	SSRAM Tag Signals	
SCTWay	Secondary cache tag way Signal indicating the way of the secondary cache tag SSRAM to be accessed.	Output
SCTag(25:0)	Secondary cache tag bus A 26-bit bus to read/write cache tags from/to the secondary cache tag SSRAM.	Bidirectional
SCTagChk(6:0)	Secondary cache tag check bus A 7-bit bus used to read/write ECC from/to the secondary cache tag SSRAM.	Bidirectional
SCTOE*	Secondary cache tag output enable A signal that enables the outputs of the secondary cache tag SSRAM.	Output
SCTWr*	Secondary cache tag write enable A signal that enables writing the secondary cache tag SSRAM.	Output
SCTCS*	Secondary cache tag chip select A signal which enables the secondary cache tag SSRAM.	Output

* All cache static RAM (SRAM) are synchronous SRAM (SSRAM).

3.3 System Interface Signals

Table 3-3 presents the R10000 processor System interface signals.

Table 3-3 System Interface Signals

Signal Name	Description	Type
System Clock Signals		
SysClk SysClk*	System clock Complementary system clock input.	Input
SysClkRet SysClkRet*	System clock return Complementary system clock return output used for termination of the system clock.	Output
System Arbitration Signals		
SysReq*	System request The processor asserts this signal when it wants to perform a processor request and it is not already master of the System interface.	Output
SysGnt*	System grant The external agent asserts this signal to grant mastership of the System interface to the processor.	Input
SysRel*	System release The master of the System interface asserts this signal for one SysClk cycle to indicate that it will relinquish mastership of the System interface in the following SysClk cycle.	Bidirectional
System Flow Control Signals		
SysRdRdy*	System read ready The external agent asserts this signal to indicate that it can accept processor read and upgrade requests.	Input
SysWrRdy*	System write ready The external agent asserts this signal to indicate that it can accept processor write and eliminate requests.	Input
System Address/Data Bus Signals		
SysCmd(11:0)	System command A 12-bit bus for transferring commands between processor and the external agent.	Bidirectional
SysCmdPar	System command bus parity Odd parity for the system command bus.	Bidirectional
SysAD(63:0)	System address/data bus A 64-bit bus for transferring addresses and data between R10000 and the external agent.	Bidirectional
SysADChk(7:0)	System address/data check bus An 8-bit ECC bus for the system address/data bus.	Bidirectional
SysVal*	System valid The master of the System interface asserts this signal when it is driving valid information on the system command and system address/data buses.	Bidirectional

Table 3-3 (cont.) System Interface Signals

Signal Name	Description	Type
	System State Bus Signals	
SysState(2:0)	System state bus A 3-bit bus used for issuing processor coherency state responses and also additional status indications.	Output
SysStatePar	System state bus parity Odd parity for the system state bus.	Output
SysStateVal*	System state bus valid The processor asserts this signal for one SysClk cycle when issuing a processor coherency state response on the system state bus.	Output
	System Response Bus Signals	
SysResp(4:0)	System response bus A 5-bit bus used by the external agent for issuing external completion responses.	Input
SysRespPar	System response bus parity Odd parity for the system response bus.	Input
SysRespVal*	System response bus valid The external agent asserts this signal for one SysClk cycle when issuing an external completion response on the system response bus.	Input
	System Miscellaneous Signals	
SysReset*	System reset The external agent asserts this signal to reset the processor.	Input
SysNMI*	System non-maskable interrupt The external agent asserts this signal to indicate a non-maskable interrupt.	Input
SysCorErr*	System correctable error The processor asserts this signal for one SysClk cycle when a correctable error is detected and corrected.	Output
SysUncErr*	System uncorrectable error The processor asserts this signal for one SysClk cycle when an uncorrectable tag error is detected.	Output
SysGblPerf*	System globally performed The external agent asserts this signal to indicate that all processor requests have been globally performed with respect to all external agents.	Input
SysCyc*	System cycle The external agent may use this signal to define a virtual System interface clock in a hardware emulation environment.	Input

3.4 Test Interface Signals

Table 3-4 presents the R10000 processor test interface signals.

Table 3-4 Test Interface Signals

Signal Name	Description	Type
	JTAG Signals	
JTDI	JTAG serial data input Serial data input.	Input
JTDO	JTAG serial data output Serial data output.	Output
JTCK	JTAG clock Clock input.	Input
JTMS	JTAG mode select Mode select input.	Input
	Miscellaneous Test Signals	
TCA	Testability control A (for manufacturing test only) This signal must be tied to Vss, through a 100 ohm resistor.	Input
TCB	Testability control B (for manufacturing test only) This signal must be tied to Vss, through a 100 ohm resistor.	Input
PLLDis	PLL disable (for manufacturing test only) This signal must be tied to Vss.	Input
PLLRC	PLL Control Node (for manufacturing test only) There must be no connection made to this signal.	
PLLSpare(1:4)	These four pins must be tied to Vss.	
Spare(1,3)	These two pins must be tied to Vss, through a 100 ohm resistor.	
TriState	Tristate Control The system asserts this signal to tristate all outputs and input/output pads except for SCClk, SCCLK*, and JTDO.	Input
SelDVCO	Select differential VCO (for manufacturing test only) This signal must be tied to Vss.	Input